Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 6, 10, 15, 19 and 23 have been amended. Claims 3, 12 and 21 have been previously cancelled. Therefore, claims 1-2, 4-11, 13-20 and 22-25 are presented for examination.

In the Office Action, claims 1, 6, 10, 15, 19 and 23 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 6, 10, 15, 19 and 23 have been amended to appear in proper condition for allowance.

Claims 1-2, 4-7, 10-11, 13-16, 19-20 and 22-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Benson (U.S. Patent No. 5,301,325) in view of Gosling (U.S. Patent No. 5,668,999). Applicants submit that the present claims are patentable over Benson in view of Gosling.

Benson discloses a code translator, constructed similar to a compiler, that accepts as an input to be translated from the assembly code written for an architecture, and produces as an output object code for a different architecture. See Benson at Abstract. Benson further discloses that during the translation an error in the source code is indicated in response to having multiple flow paths to the same block found in the code. See Benson at col. 4, ll. 58-66. Benson further discloses that another source code error is indicated if the stack depth of the initial stack and the stack depth of ending stack are different. See Benson at col. 13, ll. 52-56.

Gosling discloses a verifier for use in conjunction with programs utilizing data type specific bytecodes for verifying the proper operation of an executable program prior to actual execution by a host processor. The verifier includes a virtual stack for temporarily storing

stack information which parallels typical stack operations required during the execution of a bytecode program. See Gosling at Abstract.

Claim 1 of the present application recites signaling an error if resources of an architectural stack needed for a block of code are not available. Applicants submit that neither Benson nor Gosling discloses or suggests signaling an error if resources of an architectural stack needed for a block of code are not available. Instead, Benson discloses reporting an error message in response to the detection of having multiple flow paths to the same block or in response to having different stack depths. See Benson at col. 4, ll. 60-63 and col. 13 ll. 52-54. However, nowhere does Benson disclose or suggest signaling an error if resources of an architectural stack needed for a block of code are not available. In addition, nowhere does Gosling disclose or suggest signaling an error if resources of an architectural stack needed for a block of code are not available. Since neither Benson nor Gosling disclose or suggest signaling an error if resources of an architectural stack needed for a block of code are not available, any combination of Benson and Gosling would also not disclose or suggest the feature. Therefore, claim 1 is patentable over Benson in view of Gosling.

Claims 2 and 4-9 depend on claim 1 and contain additional features, thus claims 2 and 4-9 are also patentable over Benson in view of Gosling.

Claim 10 recites signaling an error if resources of an architectural stack needed for a block of code are not available. Thus, for the reasons described above with respect to claim 1, claim 10 is also patentable over Benson in view of Gosling. Since claims 11 and 13-18 depend on claim 10 and contain additional features, claims 11 and 13-18 are also patentable over Benson in view of Gosling.

Claim 19 recites signaling an error if resources of an architectural stack needed for a block of code are not available. Thus, for the reasons described above with respect to claim 1, claim 19 is also patentable over Benson in view of Gosling. Since claims 20 and 22-25 depend on claim 19 and contain additional features, claims 20 and 22-25 are also patentable over Benson in view of Gosling.

Claims 8-9, 17-18 and 25 stand rejected under 5 U.S.C. §103(a) as being unpatentable over Benson and Gosling as applied to claims 1, 10 and 19 respectively, and further in view of Yellin et al. (U.S. Patent No. 5,740,441). Applicants submit that the present claims are patentable over any combination of Benson, Gosling and Yellin.

Yellin discloses a program interpreter for computer programs written in a bytecode language, which uses a restricted set of data type specific bytecodes. See Yellin at Abstract. However, Yellin does not disclose or suggest signaling an error if resources of an architectural stack needed for a block of code are not available.

As discussed above, neither Benson nor Gosling disclose or suggest such a feature. Since neither Benson, Gosling nor Yellin disclose or suggest signaling an error if resources of an architectural stack needed for a block of code are not available, any combination of Benson, Gosling and Yellin would not disclose or suggest the feature. Therefore, the present claims are patentable over Benson and Gosling in view of Yellin.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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